LISTING OF CLAIMS

1. (Currently amended) A method of fabricating a shallow trench isolation feature comprising the steps of:

providing a semiconductor substrate;

forming a polysilicon polish stop layer over the semiconductor substrate;

forming a nitride containing layer over the polish stop layer;

forming a shallow trench layer through a portion of the nitride containing layer, a portion of the polish stop layer and a portion of the semiconductor substrate;

removing the nitride containing layer by a chemical mechanical polishing process; ~~and~~

planarizing the shallow trench layer and the polish stop layer until a surface of the shallow trench layer and a surface of the polish stop layer are co-planar; and

after planarizing, oxidizing substantially all of the polish stop layer to convert the polish stop layer to a field oxide layer.

2. (Original) A method according to claim 1, including the step of:

forming a barrier layer over the semiconductor substrate.

3. (Original) A method according to claim 1, including the step of:

etching an aperture through the nitride containing layer to expose a portion of the polish stop layer.

4. (Currently amended) A method according to claim 1, ~~including the steps of:~~ wherein forming the shallow trench layer includes:

forming a shallow trench through a portion of the polish stop layer and a portion of the semiconductor substrate; and

depositing an oxide in the shallow trench to form the shallow trench layer.

5-7. (Canceled)

8. (Currently amended) A method according to claim 3, wherein the nitride containing layer is at least one of Si_3N_4 ~~and~~ or SiO_xN_y.

9. (Original) A method according to claim 1, including the step of:

forming a liner layer interposed between the shallow trench layer and the semiconductor substrate.

10-20. (Canceled)

21. (New) The method of claim 1, further comprising removing the field oxide layer, wherein removing the field oxide layer includes removing a portion of the shallow trench layer so that a resulting upper surface of the shallow trench layer is co-planar with an upper surface of the semiconductor substrate.

22. (New) The method of claim 21, wherein removing the field oxide layer includes removing a barrier layer formed between the semiconductor substrate and the polish stop layer.

23. (New) A method of fabricating a shallow trench isolation feature comprising the steps of:

providing a semiconductor substrate;

forming a silicon carbide polish stop layer over the semiconductor substrate;

forming a nitride containing layer over the polish stop layer;

forming a shallow trench layer through a portion of the nitride containing layer, a portion of the polish stop layer and a portion of the semiconductor substrate;

removing the nitride containing layer by a chemical mechanical polishing process; and

planarizing the shallow trench layer and the polish stop layer until a surface of the shallow trench layer and a surface of the polish stop layer are co-planar.

24. (New) The method according to claim 23, further comprising forming a barrier layer between the semiconductor substrate and the polish stop layer.

25. (New) The method according to claim 23, further comprising etching an aperture through the nitride containing layer to expose a portion of the polish stop layer.

26. (New) The method according to claim 23, wherein forming the shallow trench layer includes:

forming a shallow trench through a portion of the polish stop layer and a portion of the semiconductor substrate; and

depositing an oxide in the shallow trench to form the shallow trench layer.

27. (New) The method according to claim 23, wherein the nitride containing layer is at least one of Si_3N_4 or SiO_xN_y.

28. (New) The method according to claim 23, further comprising forming a liner layer interposed between the shallow trench layer and the semiconductor substrate.